

ABSTRACT OF THE DISCLOSURE

A collector voltage of a power management semiconductor device is detected by a first comparator, and when the detected collector voltage exceeds a first reference voltage, the first comparator outputs a first detection signal. Furthermore, a gate voltage of the power management semiconductor device is detected by a second comparator, and when the detected gate voltage exceeds a second reference voltage, the second comparator outputs a second detection signal. The second reference voltage is a minimum gate voltage for feeding a rated power to the power management semiconductor device or over, and less than a line power voltage of a drive circuit of the power management semiconductor device. When both the first detection signal and second detection signal are being outputted, the gate voltage is reduced by a gate voltage reduction means so as to protect the power management semiconductor device from overcurrent and overvoltage.